Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1-4. (Cancelled).

5. (Currently Amended) A core logic chip for use in a personal computer system comprising a system memory and a display, said core logic chip being incorporated therein:

a graphics accelerator ~~in communication with said display, processing and outputting image data to said display~~;

a primary memory control circuit in communication with said graphics accelerator, controlled by said graphics accelerator to assert a first read/write signal;

a first data transmission channel in communication with said primary memory control circuit and said system memory, transmitting said first read/write signal to said system memory;

a backup memory control circuit in communication with said graphics accelerator, controlled by said graphics accelerator to assert a second read/write signal; and

a second data transmission channel in communication with said backup memory control circuit and said system memory, transmitting said second read/write signal to said system memory,

wherein each of said first and said second read/write signals is a part of a specific read/write signal for obtaining a specified image data from said system memory to be processed by said graphics accelerator.

6. (Currently Amended) The core logic chip according to claim 5 wherein ~~said second portion of~~ said system memory includes a frame buffer where said image data is stored.

7. (Original) The core logic chip according to claim 5 wherein said system memory is a dynamic random access memory.

8. (Original) The core logic chip according to claim 5 wherein said first and second data transmission channels are separate from each other but cooperating to transmit said specific read/write signal.

9. (New) A core logic chip for use in a personal computer system comprising a system memory and a display, said core logic chip being incorporated therein:

a graphics accelerator;

a primary memory control circuit coupled to said graphics accelerator and accessible to a frame buffer in said system memory at a request of said graphics accelerator;

a backup memory control circuit coupled to said graphics accelerator and accessible to said frame buffer in said system memory at said request of said graphics accelerator;

a first data transmission disposed between said primary memory control circuit and said system memory and transmitting a first portion of an image data from said frame buffer in response to a first read/write signal issued by said primary memory control circuit; and

a second data transmission channel disposed between said backup memory control circuit and said system memory and transmitting a second portion of said image data from said frame buffer in response to a second read/write signal issued by said backup memory control circuit.